### Sunday, March 6, 2011

**Tutorial Session**  
*Location: Atkinson Hall – Calit2 Auditorium*

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<th>Time</th>
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| 12:30 pm- 5:00 pm | M. Quershi, IBM Research  
S. Gurumurthi, University of Virginia  
B. Rajendran, IBM Research  
System Design with Phase Change Memory – Fundamentals, Opportunities and Challenges |
| 6:00 pm- 9:00 pm | Reception at the Sheraton Hotel – *The Wind and Sea Ballroom*** |

### Monday, March 7, 2011

**Continental Breakfast at Atkinson Hall - Calit2 Pre-Function Area**

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<th>Time</th>
<th>Event</th>
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<tr>
<td>8:00 am- 8:45 am</td>
<td>Opening Remarks – <em>Calit2 Auditorium</em></td>
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| 8:45 am - 9:00 am | Keynote  
Speaker: Prof. Jehoshua (Shuki) Bruck, *Caltech*                                       |
| 10:00 am- 10:45 am | Break                                                                                     |
| 10:45 am- 12:05 pm | Session I – Devices (Part 1)  
*Session Chair: Yoichiro Tanaka, Toshiba*  
*Location: Atkinson Hall – Calit2 Auditorium*                      |
<p>| 12:05 pm- 1:45 pm | Lunch / Poster Session at Calit2 – Atkinson Hall                                         |</p>
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<tr>
<th>Session II</th>
<th>Session III</th>
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<td><strong>ECC (Part 1)</strong>&lt;br&gt;Session Chair: Xinmiao Zhang, Case Western Reserve&lt;br&gt;Location: Calit2 Auditorium</td>
<td><strong>Architecture (Part 1)</strong>&lt;br&gt;Session Chair: John Davis, Microsoft Research&lt;br&gt;Location: CSE Bldg., Room 1202</td>
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<tr>
<td>Error Characterization for NAND Flash Memories&lt;br&gt;Yu Cai(^1), Erich F. Haratsch(^2), Ken Mai(^3)&lt;br&gt;DSSC, Carnegie Mellon University(^4), LSI Corporation(^2)</td>
<td>Janus-FTL: Finding the Optimal Point on the Spectrum Between Page and Block Mapping Schemes&lt;br&gt;Hunki Kwon(^1), Eunsam Kim(^2), Jongmoo Choi(^3), Donghee Lee(^1), Sam H. Noh(^2)&lt;br&gt;University of Seoul(^1), Hongik University(^2), Dankook University(^3)</td>
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<td>Some Limited Magnitude Error Correcting Codes for Flash Memories&lt;br&gt;Bella Bose(^1), Torleiv Klove(^2), Noha Elarief(^3)&lt;br&gt;Oregon State University(^4), University of Bergen(^2)</td>
<td>Sub-block Wear-leveling for NAND Flash&lt;br&gt;Roman Pletka(^1), Xiaoyu Hu(^1), Ilias Iliadis(^1), Roy Cideciyan(^1), Theodore Antonakopoulos(^2)&lt;br&gt;IBM Research, Zurich Research Lab(^1), University of Patras(^2)</td>
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<td>Error Correction Scheme for Constrained Inter-Cell Coupling in Flash Memory&lt;br&gt;Amit Berman, Yitzhak Birk&lt;br&gt;Technion - Israel Institute of Technology</td>
<td>Exploiting Memory Device Characteristics at the System Level: From Adaptive SSD to Self-Healing SSD&lt;br&gt;Tong Zhang, Qi Wu, Yangyang Pan, Guiqiang Dong&lt;br&gt;Rensselaer Polytechnic Institute</td>
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<td>Adaptive Endurance Coding for NAND Flash&lt;br&gt;Ashish Jagmohan, Michele Franceschini, Luis Lastras Montaño, John Karidis&lt;br&gt;IBM T.J. Watson Research Center</td>
<td>Leveraging Value Locality in Optimizing NAND Flash-based SSDs&lt;br&gt;Aayush Gupta, Raghav Pisolkar, Bhuvan Urgaonkar, Anand Sivasubramaniam&lt;br&gt;Pennsylvania State University</td>
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3:05 pm - 3:50 pm: Break
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<tr>
<th>Time</th>
<th>Session IV Devices (Part 2)</th>
<th>Session V Applications (Part 1)</th>
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</table>
| 3:50 pm - 5:10 pm | **Session Chair:** Janice Nickel, HP Labs  
**Location:** Calit2 Auditorium  
**Energy Efficient Circuit-System Codesign for Spin Torque Transfer Random Access Memory (STTRAM) in Submicron Technologies**  
Subho Chatterjee¹, Saibal Mukhopadhyay¹, Mitchelle Rasquinha¹, Sudhakar Yalamanchili¹, Swarup Bhunia², Somnath Paul²  
*Georgia Tech¹, Case Western Reserve²*  
**Model Based Study on Performance and Energy Optimization for STT-RAM**  
Anurag Nigam, Kamaram Munira, Avik W. Ghosh, Stuart Wolf, Mircea R. Stan  
*University of Virginia*  
**Handling PCM Resistance Drift with Device, Circuit, Architecture, and System Solutions**  
Manjunath Shevgoor¹, Manu Awasthi¹, Kshitij Sudan¹, Rajeev Balasubramonian¹, Bipin Rajendran², Viji Srinivasan²  
*University of Utah¹*, *IBM²*  
**Probabilistic Programming of STT-MTJ Clusters**  
Wenqing Wu, Xiaochun Zhu, Seung Kang, Kendrick Yuen, Matt Nowak, Jeff Levin, Rob Gilmore, Nick Yu  
*Qualcomm Inc.*  | **Session Chair:** Al Bouchers, Google  
**Location:** CSE Bldg., Room 1202  
**SSDAlloc:** Hybrid SSD/RAM Memory Management Made Easy  
Anirudh Badam, Vivek S. Pai  
*Princeton University*  
**Pathological Behavior of SSDs and Application in HPC Storage**  
Youngjae Kim¹, Junghiee Lee², Galen M. Shipman¹  
*Oak Ridge National Laboratory¹, Georgia Institute of Technology²*  
**ChunkStash:** Speeding up Storage Deduplication using Flash Memory  
Sudipta Sengupta¹, Jin Li¹, Biplob Debnath²,  
*Microsoft Research¹*, *Univ. of Minnesota²*  
**Opportunities and Challenges of Using Solid State Drives in Large Scale Datacenters**  
Badriddine Khessib, Kushagra Vaid, Sriram Sankar, Mark Shaw  
*Microsoft* |
| 6:00 pm – 9:00 pm | **Dinner at the Sheraton Hotel – The Executive Ballroom** |
**Tuesday, March 8, 2011**

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<tr>
<td>8:15 am-9:00 am</td>
<td>Continental Breakfast at Atkinson Hall - Calit2 Pre-Function Area</td>
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| 9:00 am-10:00 am | Keynote Speaker: Implications of Storage Class Memories (SCMs) on Software Architecture  
Dr. C. Mohan, IBM Almaden Research Center  |
| 10:00 am-10:45 am | Break                                                                                                   |
| 10:45 am-12:05 pm | **Session VI**  
**Architecture (Part 2)**  
Session Chair: Peter Desnoyers, Northeastern University  
Location: Calit2 Auditorium  |
|                | Advances in Wear Leveling for Storage Class Memories  
Moinuddin K. Qureshi, Michele Franceschini, Luis Lastras Montaño, John P. Karidis  
*IBM T.J. Watson Research Center*  |
|                | Moneta: A High-performance Storage Array Architecture for Next-generation, Non-volatile Memories  
Adrian M. Caulfield, Arup De, Joel Coburn, Todor I. Mollov, Rajesh K. Gupta, Steven Swanson  
*University of California, San Diego*  |
|                | PTRIM + EXISTS: Exposing New FTL Primitives to Applications  
David Nellans, Michael Zappe, Jens Axboe, David Flynn  
*FusionIO*  |
|                | Designing with STT-RAM: From Disks to Dies  
Clinton W. Smullen, IV; Sudhanva Gurumurthi  
*University of Virginia*  |
| 12:05 pm-1:15 pm | Lunch / Poster Session at Calit2 – Atkinson Hall                                                       |
| 10:45 am-12:05 pm | **Session VII**  
**ECC (Part 2)**  
Session Chair: Cai Kui, DSI / A-Star  
Location: CSE Bldg., Room 1202  |
|                | Sum Capacity of the Multiple-Write Memory  
Lele Wang, Minghai Qin  
*University of California, San Diego*  |
|                | FREE-p: Protecting Non-Volatile Memory Against both Hard and Soft Errors  
Doe Hyun Yoon¹, Naveen Muralimanohar², Jichuan Chang², Parthasarathy Ranganathan², Norman P. Jouppi², Mattan Erez¹  
*The University of Texas at Austin¹, Hewlett-Packard Labs²*  |
|                | Coding for Limiting Current in Memristor Crossbar Memories  
Erik Ordentlich¹, Gilberto Ribeiro¹, Ron M. Roth², Gadiel Seroussi¹, Pascal O. Vontobel¹  
*HP Labs¹, Technion and HP Labs²*  |
|                | Coding with Side Information for Flash Memory Endurance  
Euiseok Hwang, Seungjune Jeon, Rohit Negi, B. V. K. Vijaya Kumar  
*Carnegie Mellon University*  |
### Session VIII
#### Applications (Part 2)
**Session Chair: James Nunez, Los Alamos National Lab.**
**Location: Calit2 Auditorium – Atkinson Hall**

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<tr>
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| 1:15 pm-2:35 pm | Storage Systems for Storage-Class Memory  
Haris Volos, Michael Swift  
*University of Wisconsin*  
Redesigning Data Structures for Non-Volatile Byte-Addressable Memory  
Shivaram Venkataraman\(^1\), Niraj Tolia\(^2\), Parthasarathy Ranganathan\(^3\),  
Roy H. Campbell\(^1\)  
*University of Illinois, Urbana-Champaign\(^1\), Maginatics\(^2\), HP Labs, Palo Alto\(^3\)*  
Traversing Massive Graphs with NAND Flash  
Roger Pearce\(^1\), Maya Gokhale\(^2\), Nancy M. Amato\(^1\)  
*Texas A&M University\(^1\), Lawrence Livermore National Laboratory\(^2\)*  
Database Software For Non-Volatile Byte-Addressable Memory  
Harumi Kuno, Goetz Graefe  
*HP Labs* |
| 2:35 pm-2:50 pm | Break                                                                |
| 2:50 pm-4:50 pm | Tour - Calit2 Technology Laboratories                                |