A 7.8MB/s 64Gb 4-Bit/Cell NAND Flash Memory on 43nm CMOS Technology

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Outline

- Introduction
- 4-Bit/Cell (16LC) Distribution
- Performance Features
- Silicon Results
- Summary of Key Features
- Conclusion
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- Introduction
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Memory Density Trend

- Memory density previously reported
- 64Gb X4 provides a 2 times density improvement

Note: D# = # bits per cell
## Comparison with Previous Works

<table>
<thead>
<tr>
<th></th>
<th>43nm 16Gb D2</th>
<th>43nm 64Gb X4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>(K. Kanda, et al., ISSCC ‘08)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Chip Size</strong></td>
<td>120 mm²</td>
<td>244.5 mm²</td>
</tr>
<tr>
<td><strong>Density</strong></td>
<td>133 Mb/mm²</td>
<td>262 Mb/mm²</td>
</tr>
<tr>
<td><strong>Architecture</strong></td>
<td>8 Gb / plane</td>
<td>32 Gb / plane</td>
</tr>
<tr>
<td><strong>MLC</strong></td>
<td>4LC</td>
<td>16LC</td>
</tr>
<tr>
<td><strong>Program/Sense</strong></td>
<td>ABL</td>
<td>ABL</td>
</tr>
</tbody>
</table>

64Gb is highest capacity single die reported!

(Drawings not to scale)
Comparison with 3Xnm Products

<table>
<thead>
<tr>
<th>Device</th>
<th>32Gb D2</th>
<th>64Gb X4</th>
<th>32Gb D3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>34nm</td>
<td>43nm</td>
<td>32nm</td>
</tr>
<tr>
<td>Die Size</td>
<td>172mm²</td>
<td>244.5mm²</td>
<td>113mm²</td>
</tr>
<tr>
<td>Density Comparison</td>
<td>186Mb/mm²</td>
<td>262Mb/mm²</td>
<td>283Mb/mm²</td>
</tr>
</tbody>
</table>

R. W. Zeng, et al., ISSCC '09

This Work

T. Futatsuyama, et al., ISSCC '09
X4 Benefits

- X4 enables highest capacity
  - Expand in capacity where D2 and D3 cannot

- 2 times improvement in memory density (over previously reported works)

- Compared to published 32nm generation of technology, 43nm 64Gb X4 enables:
  - Much lower cost than 34nm D2
  - Comparable in cost effectiveness with 32nm D3
4-Bit/Cell Considerations

- More ECC parity bits to support strong ECC requirements
- Four sets of data latches
- Design challenges - 16 levels of distribution
  - Precise control of voltages and timings
  - Performance – Many levels to verify
Project Objectives

- High density in 4-bit/cell (16LC)
  - Very narrow distribution

- Performance target of 8MB/s, comparable to other MLCs Designs
  - 8MB/s D3 reported at 2008 ISSCC
    (Y. Li, et al., ISSCC ’08)
  - 9MB/s D2 reported at 2009 ISSCC
    (R. Zeng, et al., ISSCC ’09)
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Distribution Requirements

- For similar Vt window, 16LC requires much tighter distribution.

- Vt window cannot be increased too much due to device reliability considerations (Program Disturb, Read Disturb, …)

- Major obstacle in obtaining tight distribution is cell-to-cell coupling (CCC).
Cell-to-Cell Coupling

- Three components of CCC:
  - Diagonal
  - WL – WL
  - BL – BL

- CCC greatly affects final distribution width.

- With technology scaling, all 3 components of CCC increase.
Cell-to-Cell Coupling Trend

- With technology scaling, CCC increases dramatically
- To obtain tight distribution, need to overcome CCC
Issue with CCC

WL_{n+3}  
WL_{n+2}  
WL_{n+1}  
WL_n  

WL_n Distribution

Erase

WL_n Distribution (after WL_{n+1} Programming)

Erase
2-Pass Programming

- Previous Method: 2-Pass Programming
  - First pass programs roughly to lower level
  - Second pass programs to final level
  - Vth movement of second pass is small, minimizing CCC on its neighbors

N. Shibata, et al., Symp. VLSI Circuit ‘07
2-Pass Programming

Vth distribution of WL_n

(1)

Vth distribution of WL_{n+1}

(2)

(3)

(4)
2-Pass Programming

- 2-Pass is not enough to handle high CCC of technology scaling
  - CCC\(_1\) increases
    - Needs to lower \(V_{\text{Low}}\)
  - Lower \(V_{\text{Low}}\) increases \(DV_2\)
  - CCC\(_{\text{Final}}\) \(\propto\) \(DV_2\)
    - Wider distribution

- Improved algorithm to achieve tight distribution
  - Three-Step Programming (TSP)
Three-Step Programming (TSP)

- Each WL programming consists of 3 steps:
  - Step 1 – Program to 4 levels ($V_{\text{Low1}}$)
  - Step 2 – Program roughly to 16 levels ($V_{\text{Low2}}$)
  - Step 3 – Program to final 16 levels ($V_{\text{Tar}}$)
TSP – The Concept

**Step 1:** Program to $V_{\text{Low1}}$

Distribution after Step 1 of neighbor cells

**Step 2:** Program to $V_{\text{Low2}}$

Distribution after Step 2 of neighbor cells

**Step 3:** Program to $V_{\text{Tar}}$

Distribution after Step 3 of neighbor cells
TSP – Programming Sequence

Vth distribution of WL\textsubscript{n}

**Step 1:** Program to 4 levels ($V_{\text{Low1}}$)
Distribution after Step 1 of neighbors

**Step 2:** Program to 16 levels ($V_{\text{Low2}}$)
Distribution after Step 2 of neighbors

**Step 3:** Program 16 levels to $V_{\text{Tar}}$
Distribution after Step 3 of neighbors
TSP – Benefits

- Additional step minimizes the effect of CCC
  - Cell Vt movement during each step is small, reducing CCC of its neighbors.
  - $V_{\text{Low2}}$ of 2nd step can be closer to $V_{\text{Tar}}$ of 3rd step.
  - Cell Vt movement during last step is minimal and has negligible effect on its neighbors.
  - TSP reduces CCC effect to ~ 5%.

- Allows bigger programming step size during 1st & 2nd steps
  - Minimal impact on programming time
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Performance Techniques

- Performance enhancement techniques:
  - All BitLine (ABL) architecture
  - Optimization of Verification Matrix
  - Optimization of internal timing and operations
    » Cell Source noise tracking
    » WL noise cancellation

- ABL is the main reason for achieving our performance objective.

- Sequential Sense Concept (SSC) further improves performance of both read and verify operations.
Performance Comparison

This Work
43nm

7.8 MB/s

ABL
8KB Page
Sequential Sense
Optimization
- Verification Matrix
- Internal Timing & Operations

12.6 X

70nm 16Gb X4
N. Shibata, et al.,
Symp. VLSI Circuit ‘07

0.62 MB/s

This Work
43nm

7.8 MB/s

ABL
8KB Page
Sequential Sense
Optimization
- Verification Matrix
- Internal Timing & Operations

12.6 X

70nm 16Gb X4
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Symp. VLSI Circuit ‘07

0.62 MB/s
ABL Architecture

(R. Cernea, et al., ISSCC '08)

- Conventional Even / Odd architecture
  - One Sense Amplifier handling two bitlines
  - Alternating bitlines shielded during sensing

- ABL architecture
  - Simultaneous Read and Program of all bitlines
  - No shielding necessary
Sequential Sense Concept (SSC)

- Fixed sensing order from start to final levels
- For each read and verify sequence, charging of un-selected WLs and Select gates is done only once
  - WL stabilization time is minimized
- Same sequence is used for both read and verify
  - Matching of read and verify conditions
- Less Source Line (SL) current (see example next page)
Example: Sensing level 8 (WL potential = Level 8)

- Conventional sensing, cells of levels 0 – 7 are on
- With SSC, only cells of level 7 are on
- SSC generates less SL current
  - Smaller SL bounce
  - Less SL stabilization time
  - Less current consumption
Sequential Sense Concept (SSC)

- After sensing of level 8 is complete, page (0) data is available for shifting out.
- After sensing of level C, page (1) data is available; after level E, page (2) data is ready.
- With SSC, data can be shifted out in parallel with internal sensing, supporting cache operation.
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16LC Distribution

- Measured Distribution of 16 LC
- Tight distribution is achieved with TSP
Performance

- Total Tprog for 3 steps = 8.41ms
- 7.8MB/s with 2-plane (16KB x 4) programming
  - ABL is the main contributor to high performance
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Summary of Key Features

- 43nm CMOS Flash technology
- 64Gb, 4-bit/cell
- ABL with 2-sided SA
- Organization
  - Dual Plane array
  - 32Gb / plane
  - 2K blocks / plane
  - Block size = 16Mb (4M cells)
  - 66 NAND string
  - 8KB page size
## Summary of Key Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture</td>
<td>ABL</td>
</tr>
<tr>
<td>Write Throughput</td>
<td>7.8MB/s</td>
</tr>
<tr>
<td>Tprog (per page)</td>
<td>2.1ms</td>
</tr>
<tr>
<td>Tread (per page)</td>
<td>60us</td>
</tr>
<tr>
<td>Terase</td>
<td>3ms</td>
</tr>
<tr>
<td>Burst Cycle Time</td>
<td>25ns</td>
</tr>
<tr>
<td>Power Supply</td>
<td>2.7 to 3.6V</td>
</tr>
<tr>
<td>Technology</td>
<td>3-Metal 43nm</td>
</tr>
<tr>
<td>Die Size</td>
<td>244.45 mm²</td>
</tr>
</tbody>
</table>
Conclusion

- A high performance 64Gb 4-bit/cell is reported.
  - Developed on 43nm CMOS technology
  - Highest capacity ever reported

- 16LC tight distribution is achieved with TSP.

- Able to achieve performance on par with other MLC designs by leveraging:
  - ABL architecture
  - Sequential Sense Concept (SSC)
  - Extensive optimization of verification matrix and internal operations
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