Toggle and Torque: MRAM at Everspin Technologies

Nick Rizzo
Everspin introduction

- The leading developer and manufacturer of integrated magnetic products.
  - Industry-first MRAM manufacturer since June 2006
  - Embedded MRAM systems: 1st SOC into production in 2010
  - Integrated magnetic sensors: 1st integrated system in 2010

- Formed as Everspin in June 2008 – Previously part of Freescale Semiconductor

- Expanded portfolio to 50 products currently
  - Focus on innovation, quality, cost, reliability, manufacturability
## Current MRAM portfolio

### 16-bit I/O

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Density</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR4A16B</td>
<td>16Mb</td>
<td>1MX16</td>
</tr>
<tr>
<td>MR2A16A</td>
<td>4Mb</td>
<td>256Kx16</td>
</tr>
<tr>
<td>MR1A16A</td>
<td>2Mb</td>
<td>128Kx16</td>
</tr>
<tr>
<td>MR0A16A</td>
<td>1Mb</td>
<td>64Kx16</td>
</tr>
</tbody>
</table>

### 8-bit I/O

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Density</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR2A08A</td>
<td>4Mb</td>
<td>512Kx8</td>
</tr>
<tr>
<td>MR0A08B</td>
<td>1Mb</td>
<td>128Kx8</td>
</tr>
<tr>
<td>MR256A08B</td>
<td>256Kb</td>
<td>32kX8</td>
</tr>
</tbody>
</table>

### SPI I/O

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Density</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR25H10</td>
<td>1Mb</td>
<td>128Kx8</td>
</tr>
<tr>
<td>MR25H512</td>
<td>512Kb</td>
<td>64Kx8</td>
</tr>
<tr>
<td>MR25H256</td>
<td>256Kb</td>
<td>32Kx8</td>
</tr>
</tbody>
</table>

### Commercial, Industrial, Extended, Automotive

- **Commercial**: 0 to +70 °C
- **Industrial**: -40 to +85 °C
- **Extended**: -40 to +105 °C
- **Automotive**: -40 to +125 °C

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**48-BGA**
- x8 Asynchronous parallel I/O
- x16 Asynchronous parallel I/O

**44-TSOPII**
- x8 Asynchronous parallel I/O
- x16 Asynchronous parallel I/O

**8-DFN**
- SPI-compatible serial I/O
- 40 MHz; No write delay
Everspin MRAM Recognized as Industry Breakthrough Product

- 2009: Red Herring Award: Top 100 most promising tech companies
- 2008: Business Week “Most Successful Startups”
- 2008: Forbes/Wolfe Emerging Tech Reports – “companies to watch”
- 2007: Design News Golden Mousetrap Award
- 2007: R&D Magazine - Top 100 Inventions of 2007
- 2007: EE Times China Ace Award - Best Product of the Year – Memory
- 2007: Japan Embedded Systems Expo - Memory of Year
- 2007: In-Stat’s Innovation Award
- 2006: Named Product of the Year by Electronic Products
- 2004: MIT Technology Review- MRAM “Toggle” is one of 5 Killer 2003 Patents

BusinessWeek

Most Successful US Startups
Everspin Applications, Customers

Value differentiation
Non-volatile
Fast read and write
Unlimited endurance
Highly reliable

Office Automation
Consumer & gaming
Storage systems & servers
Industrial automation & robotics
Energy management
Transportation
Networking communications

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## Memory Comparison

<table>
<thead>
<tr>
<th></th>
<th>Toggle MRAM (180 nm)</th>
<th>Toggle MRAM (65 nm)*</th>
<th>ST MRAM (65 nm)*</th>
<th>FLASH (65 nm)+</th>
<th>DRAM (65 nm)+</th>
<th>SRAM (65 nm)+</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>cell size (µm²)</strong></td>
<td>1.25</td>
<td>0.16</td>
<td>0.04†</td>
<td>0.04</td>
<td>0.03</td>
<td>0.3</td>
</tr>
<tr>
<td><strong>Read time</strong></td>
<td>35 ns</td>
<td>10 ns</td>
<td>10 ns</td>
<td>10 - 50 ns</td>
<td>10 ns</td>
<td>1 ns</td>
</tr>
<tr>
<td><strong>Program time</strong></td>
<td>5 ns</td>
<td>5 ns</td>
<td>10 ns</td>
<td>0.1-100 ms</td>
<td>10 ns</td>
<td>1 ns</td>
</tr>
<tr>
<td><strong>Endurance</strong></td>
<td>&gt; 10⁻¹⁵</td>
<td>&gt; 10⁻¹⁵</td>
<td>&gt; 10⁻¹⁵</td>
<td>&gt; 10⁻¹⁵ read, &gt; 10⁵ write</td>
<td>&gt; 10⁻¹⁵</td>
<td>&gt; 10⁻¹⁵</td>
</tr>
<tr>
<td><strong>Non-volatility</strong></td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>YES</td>
<td>NO</td>
<td>NO</td>
</tr>
</tbody>
</table>

* 65nm MRAM values are projected
+ These values are from the ITRS roadmap
† This cell size only considers bit area and ignores CMOS limitations
Toggle MIRAM
Toggle MRAM Bit Cell

- Sense path electrically isolated from program path

Magnetic Tunnel Junction

ON for sensing, OFF for programming

I

H

Write Line 2

Top Electrode

I_{\text{sense}}

I_{\text{Ref}}

Write Line 1

Bottom Electrode
Toggle switching for balanced SAF

$$ M_1 = M_2 $$

- **Lower Energy to “flop” and scissor**
- **Field exceeds SAF strength**
Toggle MRAM Switching Sequence

- Phased current pulses produce rotating field
- Toggle – same field sequence always changes state of bit
Toggle bit switching

Theoretical simulation of Toggle switching

- H > H_{sat}: Doesn’t switch
- H_{sw} < H < H_{sat}: Switches
- H < H_{sw}: Doesn’t Switch

4M high speed memory test

- Operating Region
  - T = 125 ºC
  - 0 errors

- Non-Switching Region

• Threshold programming ensures high reliability
Spin Torque MRAM
Comparison of 0.18 \( \mu \text{m} \) Toggle MRAM and 65nm ST-MRAM

**Toggle MRAM:**
- likely more reliable
- in production

**ST-MRAM has potential to be:**
- higher density – (if \( J_c \) can be reduced to utilize minimum pass XTOR)
- lower write power

**Comparison:**

- **Toggle MRAM**
  - Cell size \( \approx 1 \mu \text{m}^2 \)
  - CMOS 0.18\( \mu \text{m} \)
  - \( I \approx 100 \mu \text{A} \)

- **ST-MRAM**
  - Cell size \( \approx 0.04 \mu \text{m}^2 \)
  - CMOS 65nm
Spin Torque Programming for High Density, Low Power MRAM

• Use spin momentum from current to change direction of $S$, $m$.

Fixed Layer  |  Tunnel Barrier  |  Free layer
---|---|---

Net change in $S = \hbar \text{ per } e^-$

$$\frac{\Delta S}{\Delta t} = \text{Torque}$$

Remanent loop: 100 ms $I$-pulse

$J_c \sim 10^6 - 10^7 \text{ A/cm}^2$

• Optical patterning of 0.1 µm bits
Challenge of ST-MRAM:
Reduce critical current density $J_c$

For high density:
- Low $J_c \Rightarrow$ small pass Xtor

$\bullet I_{sat} \approx 500 \mu A/\mu m$ gate width for Si XTOR

For high reliability:
- Low $J_c \Rightarrow$ no tunnel barrier breakdown

$V_{sw} \propto RA \quad V_{bd} \propto \log(RA)$

$V_{applied}$

Need $> 12\sigma$ separation

Lower the RA until minimum
Breakdown voltage ($V_{bd}$) vs. $RA$ comparison

- quasistatic $V_{bd}$
- bit size $\approx 0.1 \times 0.2 \ \mu m^2$

$V_{bd}$ (V) decreases approx. logarithmically as RA decreases.
To reduce $J_c$ for spin torque switching

$$J_c \approx \left(\frac{2e}{\hbar}\right)\left(\alpha\right)\left(\frac{1}{\varepsilon}\right)\left(M_s t\right)\left(H_k + 2\pi M_s\right)$$

- Higher efficiency $\varepsilon$
- Higher MR
- Low damping ($\alpha$)
- Perpendicular $H_k$ in free layer
- Low $M_s$ and/or thinner free layer ($E_b \propto M_s V$)
- Need combination of good properties for low $J_c$

Spin torque

Time to data loss

$\tau = \tau_0 e^{\frac{E_b}{k_b T}}$
ST Switching and breakdown from 16kb CMOS arrays

- Pulse duration $t_p = 100\text{ns}$
- Bit size: $0.1\mu\text{m} \times 0.18\mu\text{m}$

- Good separation $> 12\sigma$, but need to eval. larger number of bits, more cycles

Histogram of several hundred bits in low R state switched 1000 times

- Before pulses
- After 1000 pulses (50 ns duration)

Voltage includes pass transistor
Summary

- Toggle MRAM in production (since 2006) and is a highly reliable, fast, nonvolatile memory.

- ST-MRAM has potential for higher density, lower power if $I_{sw}$ can be further reduced.
  
  • From switching kilobit CMOS arrays at $t_p = 100$ns:
    
    $<I_{sw}> \approx 0.5$ mA, $<E_b/k_bT> \approx 75$
    
    $<\sigma_{sw}> \approx 4\%$, $<\sigma_{bd}> \approx 3\%$
    
    Separation $> 12\sigma$