Embedded STT-MRAM for Mobile Applications:

*Enabling Advanced Chip Architectures*

Seung H. Kang

Qualcomm Inc.
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Qualcomm Is World’s Leader in Mobile Communication & Computing

- No. 1 Wireless Semiconductor Company
- No. 1 Fabless Semiconductor Company
- No. 6 Semiconductor Company
- ~11,900 US Patents & ~56,100 Foreign Patents (12/2009)
Mobile Computing Is a System Business

- **Apps Processor**: 1GHz core, Dual core
- **Software**: Windows Mobile, BREW, Symbian, Android
- **Modem**: CDMA2000, EV-DO, WCDMA, HSPA, CDMA2000, GSM, GPRS, EDGE, LTE
- **Multimedia**: Audio, HD Video, 2D/3D Graphics, + More
- **RF**: WLAN 700 MHz, 800 MHz, 900 MHz, Bluetooth 1800 MHz, 1900 MHz, 2100 MHz
- **Baseband CPU**
- **Connectivity**: WLAN, Bluetooth, USB, Broadcast, SDIO
- **GPS**: Standalone Assisted
- **Memory**
- **Power Management**
Memory Positioning in System Architecture

Specification

HW/SW Partitioning

Embedded Memory (IDM & Foundry)

Process

Core

Synthesized

Hardware

Embedded Instruction Memory

Data Cache

Scratch Pad Memory

Embedded Data Memory

Off-Chip RAM

Off-Chip FLASH

HW

SW

Standalone Memory (Memory Supplier)

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Motivation for Embedded NVM

• Higher Performance
  o Higher bandwidth; Elimination of IO buffers

• Lower Power
  o Elimination of capacitive load from the external bus and IO buffers
  o No static power dissipation from the array

• Lower System Cost
  o Reduced packaging cost and/or elimination of external memory
  o Mitigating pad-limited designs

• Custom Memory Design to Optimize the System
  o Competitive architectural advantages (product differentiator)

• Security

Due to cost, there is a desirable window of embedded memory density. Embedded NVMs are not considered to replace standalone NVMs for high-density applications.
eFLASH for Mobile SOC Applications?

In general, eFLASH is not suitable for mobile chip applications

- Technology Node Gap
  - *eFLASH lags behind the leading logic technology by ~3 generations*

- Not a Logic-Friendly Technology
  - Process overhead: 6~8 extra masks
  - Process complexity: different types of transistors & gate oxides

- Memory Attributes Not Compelling Enough
  - High voltage operation
  - Insufficient performance (marginal advantage over the standalone option)
  - Limited reliability (endurance)

- Not a RAM: No alternative to eSRAM and eDRAM
Mobile Embedded NVM Requirements

- Performance: read & write cycle $10\text{~to~}100\text{ns}$ or better; wide IO capable
- Endurance: $>10^{12}$ cycles for RAM applications
- Low Power Logic Compatibility: 45, 32 nm, and beyond
- Cell Size & Density: less demanding requirements than standalone memory

STT-MRAM is most promising with a combination of high speed and high endurance.
Ideal Target: Nonvolatile “Working RAM/Memory”

By far, no embedded NVM exists in memory hierarchy

A nonvolatile working memory can enable a disruptive system architecture with competitive advantages versus conventional eSRAM or eDRAM solutions
45nm Low-Power Embedded STT-MRAM
Enablement Challenges

Memory cells must first meet the constraints of advanced logic technology

- Device Engineering
  - LSTP NMOS access transistor: lower $I_{on}$
  - $V_{ddcore}$: 1.1V

- Process Engineering
  - MTJ integration into porous low-k dielectric BEOL
  - Compatibility with logic BEOL thermal budget
  - MTJ size & shape distribution control

- Manufacturing Infrastructure
  - 300mm MRAM modules at a leading-edge logic fab
Technology Demonstrator
Industry’s First 45nm Embedded STT-MRAM

Lin et al. IEDM 2009 (jointly by Qualcomm & TSMC)
45 nm Switching Characteristics

Switching is thermally assisted for the pulse width $> \sim 10$ ns
Switching becomes precessional for the pulse width $< \sim 10$ ns

\[ I_c = I_{c0} \left[ 1 - \frac{k_B T}{E_B} \ln(f_0 t_p) \right] \]
## Design & Process Margin Challenges

|       | NMOS | PMOS | MTJ | T (°C) | $V_{|BL-SL|}$ (V) | $V_{WL}$ (V) |
|-------|------|------|-----|--------|------------------|--------------|
| Typical | T    | T    | T   | 25     | 1.1              | nominal      |
| Slow   | S    | S    | $+4\sigma$ | -40    | 0.99 $V_{\text{norm}}$-10% |
| Fast   | F    | F    | $-4\sigma$ | 125    | 1.21 $V_{\text{norm}}$+10% |

### Macro Design Factors
- $V_{DD}$: 1.1 V for 45nm LSTP
- $V_{WL}$
- $|V_{BL}-V_{SL}|$
- Interconnect parasitic
- Switching current asymmetry
- Voltage headroom
Read Disturb Reliability

Ensuring bit stability during read cycles at high temperatures is critical.

Equivalent to $>10^{11}$ read cycles with 10ns pulses at 125°C

Lee & Kang, Trans. Mag (2010)
MTJ Breakdown Reliability

Larger separation ($\Delta_2$) between $V_{MTJ}$ and VBD is key to higher endurance cycles

$V_{BD\_mean}$: 1.164V
$V_{BD\_std}$: 0.077V

Lin et al. IEDM (2009)
Intrinsic endurance limit should be adequate as a working memory.
Memory macros are custom designed to fit particular architectural needs. Neither a high-density embedded memory scenario nor a universal memory scenario is necessary.
Embedded STT-MRAM Opportunity: Example 1

Key Enabling Attributes: Nonvolatility, Cost, Logic Compatibility

What features can the embedded STT-MRAM provide?
- Modem system software
- Secondary boot loader
- Nonvolatile scratch pad (in lieu of the external PSRAM)

- Significant power savings attributed to the absence of EBI power for MCP
- Significant cost savings due to the elimination of MCP and simpler system architecture
Embedded STT-MRAM Opportunity: Example 2

Key Enabling Attributes: Cost, Static Power, Logic Compatibility

- ~3 times smaller area achievable by embedded STT-MRAM at 45 nm
- No static power is dissipated (zero leakage) from the memory array

Non-Volatile Memories Workshop, UCSD, April 11-13, 2010
Embedding STT-MRAM Opportunity: Example 3

Key Enabling Attributes: Nonvolatility, Performance, Logic Compatibility

- Enable true instant-on and -off (memory power can be shut down)
- Fast warm- and cold-booting: enhanced user experience
More than Memory: Nonvolatile Logic

Key Enabling Attributes: Nonvolatility, Reprogrammability, Logic Compatibility

Nonvolatile LUT formed in STT-driven MTJs
Suzuki et al. (Tohoku Univ. & Hitachi), VLSI Symp. (2009)

Improving the write performance and enabling the design environment are the keys to successful implementation

Non-Volatile Memories Workshop, UCSD, April 11-13, 2010
Embedded STT-MRAM & Reconfigurable Logic

3-D Stacked Reconfigurable Logic

Reconfigurable SOC

- Key to Success
  - High TMR for STT-Logic & low switching power for STT-MRAM
  - MTJ materials & device engineering
  - System architecture optimization: performance & power

Sekikawa et al. IEDM (2008)
Summary

• High-performance and high-endurance embedded NVMs are in demand, which can bring architectural advantages for advanced low-power SOCs
  o Must bridge the technology node gap versus the leading logic

• Yet in R&D, STT-MRAM offers most desirable embedded NVM attributes
  o Performance, endurance, and logic compatibility are the key enablers
  o Further improvement in write performance is desired
  o To maximize the benefits, HW and SW architectural changes are desired

• To be adopted for a mainstream SOC, embedded STT-MRAM must be productized *timely* at the leading-edge logic node
  o Need a pilot product driver (at the current-level of technology maturity)
  o For future, explore “More-Than-Moore” or “Beyond-Moore” opportunities