Storage Class Memory

Towards a disruptively low-cost solid-state non-volatile memory

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Outline

▪ Motivation
  • by 2020, server-room power & space demands will be too high
  • evolution of hard-disk drive (HDD) storage and Flash cannot help
  • need a new technology – **Storage Class Memory (SCM)** – that combines
    ❖ the benefits of a solid-state memory (**high performance** and **robustness**)
    ❖ the **archival capabilities** and **low cost** of conventional HDD

▪ How could we build an SCM?
  • combine a scalable non-volatile memory
    ־ **STT-RAM?** **RRAM?** **PCM?**
  • with **ultra-high density** integration, using
    ❖ micro-to-nano addressing
    ❖ multi-level cells
    ❖ 3-D stacking

▪ Conclusion
  • With its combination of **low-cost** and **high-performance**, SCM could impact much more than just the server-room...
Power & space in the server room

The cache/memory/storage hierarchy is rapidly becoming the **bottleneck for large systems**.

We know how to create MIPS & MFLOPS cheaply and in abundance, but **feeding them with data** has become the performance-limiting **and** most-expensive part of a system (in both $ and Watts).

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**U.S. Market**

**New server spending**

**Power and cooling**

Source: IDC 2006, Document # 201722, “The Impact of Power and Cooling on Data Center Infrastructure”, John Humphreys, Jed Scaramella
...yet critical applications are also undergoing a paradigm shift

**Compute-centric paradigm**

**Main Focus:** Solve differential equations

**Bottleneck:** CPU / Memory

**Typical Examples:**
- Computational Fluid Dynamics
- Finite Element Analysis
- Multi-body Simulations

**Data-centric paradigm**

**Main Focus:** Analyze petabytes of data

**Storage & I/O**
- Search and Mining
- Analyses of social/terrorist networks
- Sensor network processing
- Digital media creation/transmission
- Environmental & economic modeling

Extrapolation to 2020

- **5.6 million HDD**
  - 19,000 sq. ft. !!
  - 25 Mega watts

- **21 million HDD**
  - 70,000 sq. ft. !!
  - 93 Mega watts

[at 90% CGR → need 8.4G SIO/sec]

[Freitas:2008]
Problem: The **access-time gap** between memory & storage

- Modern computer systems have to be carefully designed to **hide this gap**
- Lots of server-room **power** spent to keep disk-drives spinning
- With no on-chip storage, sensor (& other) data must be passed **deep into the network**
- **Slow searching** through huge databases because all the data must come off of disk first

...what if we could build a technology that could **bridge this gap**?
Storage Class Memory

A solid-state memory that blurs the boundaries between storage and memory by being low-cost, fast, and non-volatile.

**1980**
- Logic: CPU
- Memory: RAM
- Active Storage: DISK
- Archival: TAPE

**2009**
- Logic: CPU
- Memory: RAM
- Active Storage: DISK
- Archival: TAPE
- Flash SSD

**2013+**
- Logic: CPU
- Memory: RAM
- Active Storage: SCM
- Archival: TAPE

Storage Class Memory A solid-state memory that blurs the boundaries between storage and memory by being low-cost, fast, and non-volatile.
Storage-type vs. memory-type Storage Class Memory

- **Storage-type** uses low cost and high endurance.
- **Memory-type** uses high speed and high bandwidth.

Comparison chart showing:
- **Read Latency**
  - 100ns
  - 10μs
  - 1μs
  - 10μs
  - 100μs

- **Cell size** [F²]
  - 2
  - 4
  - 6
  - 8
  - 10

- **Speed** (Latency & Bandwidth)
- **Cost/bit**
- **Power!**
- **Endurance** (Write)
A solid-state memory that **blurs the boundaries** between storage and memory by being **low-cost, fast, and non-volatile**.

- **SCM requirements for Memory (Storage) apps**
  - No more than 3-5x the **Cost** of enterprise HDD (< $1 per GB in 2012)
  - **<200nsec (<1 µsec)** Read/Write/Erase time
  - >100,000 **Read I/O operations** per second
  - >1GB/sec (>100MB/sec)
  - **Lifetime** of $10^9 - 10^{12}$ write/erase cycles
  - 10x lower **power** than enterprise HDD
Can HDD & Flash improve enough to help?

- **Magnetic hard-disk drives (HDD)**
  - **bandwidth** issues (hidden with parallelism, but at power/space cost)
  - slow **access** time (not improving, hard to hide with caching tricks)
  - **reliability** (newest drives are *less reliable* → data losses inevitable)
  - **power** consumption (must keep drives spinning to avoid even longer access times)

- **Flash**
  - slow read/write **access time** (yet processors keep getting faster)
  - low write **endurance** (<$10^6$) (need >$10^9$ for continuously streaming data)
  - block architecture
  - **scalability** beyond the end of this decade? (yes, at least until the 1X node)
NAND Scaling Road Map

- Migrating to Semi-spherical TANOS memory cell 2009
- Migrating to 3-bit cell in 2010
- Migrating to 4-bit cell in 2013
- Migrating to 450mm wafer size in 2015
- Migrating to 3D Surround-Gate Cell in 2017

Source: Chung Lam, IBM
How does SCM compare to existing technologies?

Cost

- NOR FLASH
- NAND FLASH
- DRAM
- SRAM
- HDD

Performance

- STORAGE CLASS MEMORY
Candidate device technologies

- **Improved Flash**
  - improvements would be required in write endurance & speed

- **FeRAM** – commercial product but difficult to scale!

- **MRAM** – commercial product, also difficult to scale!
  - **STT-RAM** – sacrifice infinite endurance for lower currents
  - **Racetrack memory** – new concept w/ promise, still at point of early basic physics research

- **RRAM (Resistive RAM)**
  - Organic & polymer memory
  - **Memristor**
  - **Solid Electrolyte**

- **PC-RAM (Phase-change RAM)**
**RRAM (Resistive RAM)**

- Numerous examples of materials showing hysteretic behavior in their I-V curves
- Mechanisms not completely understood, but major materials classes include:
  - Metal nanoparticles(?) in **organics**
    - Could they survive high processing temperatures?
  - Metallic filaments in **solid electrolytes**
  - Oxygen vacancies in **transition-metal oxides**
    - Tremendous progress over last few years
      → Integrated demos with <1us write, 1e6 endurance in ~50nm diameter devices
- Things I’d worry about if I worked on RRAM:
  - Need for higher-voltage forming step
  - “Switching reproducibility”
  - Bipolar operation/read-disturb vs. cross-point diode operation
  - Voltage-time dilemma (switch in 100ns, can it still retain for 10yrs?)

[Karg:2008]
Phase-change RAM

PCRAM
“programmable resistor”

Access device
(transistor, diode)

Potential headache:
High power/current
→ affects scaling!

Potential headache:
If crystallization is slow
→ affects performance!

Voltage
temperature

Bit-line

Word-line

“RESET” pulse

“SET” pulse

Temperature

T_{melt}

T_{cryst}

Time
PCM @ IBM Almaden

- Prototype memory devices
  
  3nm * 20nm → 60nm²
  ≈ Flash roadmap for 2013
  → phase-change scales

- Phase-change materials work

- Device & materials modeling

Phase-change “bridge”

W defined by lithography
H by thin-film deposition

[B. S. Lee
Science 2009]

[Chen
IEDM 2006]
PCM @ IBM Almaden

- Ultra-scaled PCM pore cells

→ PCM as a CMOS-compatible synapse

- Improvements to PCM
  - Drift of intermediate resistances
  - Interplay between stoichiometry changes & endurance (other effects)
Cost structure of silicon-based technology

Cost determined by:

- cost per wafer
- # of dies/wafer
- memory area per die [sq. μm]
- memory density [bits per 4F²]
- patterning density [sq. μm per 4F²]

### Device | Critical feature-size F | Area (F²) | Density (Gbit /sq. in)
--- | --- | --- | ---
Hard Disk | 50 nm (MR width) | 1.0 | 250
DRAM | 45 nm (half pitch) | 6.0 | 50
NAND (2 bit) | 43 nm (half pitch) | 2.0 | 175
NAND (1 bit) | 43 nm (half pitch) | 4.0 | 87
Blue Ray | 210 nm (λ/2) | 1.5 | 10

[Fontana:2004, web searches]
Need a 10x boost in density **BEYOND** Flash!

**Diagram:**
- **MRAM** (25F^2@180nm [2])
- **FeRAM** (15F^2@130nm [40])
- **PCRAM** (5.8F^2@90nm [56])
- **solid electrolyte** (4F^2@90nm [74])

**Graph:**
- **NAND**
- **NOR**

**Effective area per stored bit**
- 1 µm^2
- 0.1 µm^2
- 0.01 µm^2
- 1000 nm^2
- 100 nm^2
- 10 nm^2

**Year**
- 2000
- 2002
- 2004
- 2006
- 2008
- 2010
- 2012
- 2014
- 2016
- 2018
- 2020

**Target:**
(10x density of 2-bit MLC NAND)

**Other markers:**
- **solid electrolyte** (20nm dia. [73])
- **Phase-change** (20nm x 3nm [55])

**Line:**
- F^2 (DRAM ½ pitch)
Paths to ultra-high density memory

starting from standard $4F^2$ ...

...add $N$ 1-D sub-lithographic "fins" ($N^2$ with 2-D)

...store $M$ bits/cell with $2^M$ multiple levels

...go to 3-D with $L$ layers
MLC with PCM

- Direct write NOT sufficiently accurate
- Various schemes for iterative write
- Iterative write works, but
  - latency, endurance impact?
  - errors despite fixed # of iterations?

2:30pm Luis Lastras Montano
2:50pm Michele Franceschini

- Drift of resistance states
3-D stacking of PCM

Intel/Numonyx: use 2nd amorphous PCM-like material as threshold switch

- similar material to PCM
- simply stack on PCM

but...

- readout by breakdown, so → read-reinforce SET, but destructive read of MLC?
- high read-currents → bandwidth?
- half-select leakage? (linear plots?)

IBM Almaden: PCM-capable access device

→ to appear in VLSI Technology Symposium, June 2010
If you could have SCM, why would you need anything else?

- $100k / GB
- $10k / GB
- $1k / GB
- $100 / GB
- $10 / GB
- $1 / GB
- $0.10 / GB
- $0.01 / GB

SCM

Chart courtesy of Dr. Chung Lam
IBM Research
Updated version of plot from IBM Journal R&D article
Conclusions

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For more information…


Thank you!